WHAT IS CLAIMED IS

1. A semiconductor memory device comprising:

a first word line;

a second word line which extends in parallel to said first word line;

word line activation signal line means which extends perpendicularly to said first and second word lines;

a device isolation region which extends perpendicularly to said first and second word lines;

a first driver for activating said first word line, said first driver comprising a first impurity region provided adjacent to said device isolation region and connected to said word line activation signal line means, a first gate electrode, and a second impurity region connected to said first word line;

a second driver for activating said second word line, said second ~~driving~~ driver comprising a third impurity region provided adjacent to said device isolation region on an opposite side from the first impurity region and connected to said word line activation signal line means, a second gate electrode, and a fourth impurity region connected to said second word line; and

a decoder connected to the first and second gate electrodes.

2. The semiconductor memory device as claimed in claim 1, wherein said word line activation signal line means includes first and second boost signal lines one of which transfers a word line activation signal at

one time, said first impurity region of said first driver being connected to the first boost signal line, said third impurity region of said second driver being connected to the second boost signal line.

3. The semiconductor memory device as claimed in claim 2, wherein said device isolation region is provided at an intermediate position between the first and second boost signal lines.

4. The semiconductor memory device as claimed in claim 2, wherein said first and second drivers are arranged within a specific region defined by the first and second boost signal lines, and said decoder is provided outside the specific region on an outer side of the second boost signal line.

5. The semiconductor memory device as claimed in claim 4, which further comprises a memory cell array which is connected to said first and second word lines, said memory cell array being provided outside the specific region on an outer side of the first boost signal line.

6. The semiconductor memory device as claimed

in claim 1, wherein said first driver includes two said first impurity regions and two said first gate electrodes, and said second driver includes two said third impurity regions and two said second gate electrodes, said first impurity regions and said first gate electrodes surrounding said second impurity region from both sides, said third impurity regions and said second gate electrodes surrounding said fourth impurity region from both sides.

7. The semiconductor memory device as claimed in claim 1, wherein said first driver includes two said first impurity regions, said second driver includes two said third impurity regions, said first gate electrode has an approximate U-shape surrounding said second impurity region, and said second gate electrode has an approximate U-shape surrounding said fourth impurity region.

8. The semiconductor memory device as claimed in claim 1, wherein said word line activation signal line means includes a single signal line which transfers a word line activation signal, and said first impurity region of said first driver is connected to the signal line.

9. The semiconductor memory device as claimed in claim 8, wherein said first driver is provided at an intermediate position between the signal line and said

device isolation region.

10. The semiconductor memory device as claimed in claim 8, wherein said decoder is provided on one side of said second driver opposite to said device isolation region.

11. The semiconductor memory device as claimed in claim 10, which further comprises a memory cell array which is connected to said first and second word lines, said memory cell array being provided on an outer side of the signal line opposite to said first driver.

12. The semiconductor memory device as claimed in claim 8, wherein said first driver includes two said first impurity regions, said second driver includes two said third impurity regions, said first gate electrode has an approximate U-shape surrounding said second impurity region, and said second gate electrode has an approximate U-shape surrounding said fourth impurity region.

13. The semiconductor memory device as claimed in claim 1, which further comprises first and

second element regions which extend perpendicularly to said first and second word lines on both sides of said device isolation region, said first driver being provided within said first element region, said second driver being provided within said second element region.

14. The semiconductor memory device as claimed in claim 13, wherein said first and second word lines form a first pair, said first and second drivers form a second pair, a plurality of the first pairs are arranged in a direction ~~parallel~~ perpendicular to said word line activation signal line means, and a plurality of the second pairs are arranged in the direction ~~parallel~~ perpendicular to said word line activation signal line means, each of said first drivers of the second pairs being formed within said first element region, each of said second drivers of the second pairs being formed within said second element region.

END